In the Specification

Please amend the specification of this application as follows:

Rewrite paragraph [0007] as follows:

--[0007] A first compressor "critical transistor stage path" may be defined as the path having the greatest transistor stage level between an input and an output within first compressor 200. Similarly, a first compressor "critical logic stage path" may be defined as the path having the greatest logic stage level between an input and an output within first compressor 200. Decreasing the first compressor critical transistor stage path level may increase the speed of the multiplier. Similarly, decreasing the first compressor critical logic stage path level also may increase the speed of the multiplier. However, each 4-2 compressor may have a plurality of first compressor critical transistor stage paths and a plurality of first compressor critical logic stage paths, or alternatively, may have a single first compressor critical transistor stage path. For ~~Example,~~ example, in compressor 200, path (A) is a first compressor critical transistor stage path and also is a first compressor critical logic stage path because for path (A), the transistor stage level is seven and the logic stage level is three, and no other paths between an input and an output have a greater transistor stage level or a greater logic stage level. Path (B) is not a first compressor critical transistor stage path because for path (B), the transistor stage level only is six, and as such, the transistor stage level for path (A) is greater than the transistor stage level for path (B). However, path (B) is a first compressor critical logic stage path because the logic stage level for path (B) is three, and as such, the logic stage level for path (B) is the same as the transistor stage level for path (A).--

Rewrite paragraph [0009] as follows:

--[0009] A successive compressor "critical transistor stage path" may be defined as the path having the greatest transistor stage level from one of the inputs of first compressor 200 to first compressor 200 carry bit output Xo and further to successive compressor 200 summation output So or carry bit output Co. Similarly, a successive compressor "critical logic stage path" may be defined as the path having the greatest logic stage level from one of the inputs of first compressor 200 to first compressor 200 carry bit output Xo and further to successive compressor 200 summation output So or carry bit output Co. Decreasing the successive compressor critical transistor stage path level may increase the speed of the multiplier. Similarly, decreasing the successive compressor critical logic stage path level also may increase the speed of the multiplier. However, each 4-2 compressor may have a plurality of successive compressor critical transistor stage paths and a plurality of successive compressor critical logic stage paths, or alternatively, may have a single successive compressor critical transistor stage path. For ~~Example,~~ example, in compressor 200, successive path (C) is a successive compressor critical transistor stage path and also is a successive compressor critical logic stage path because for successive path (C) the transistor stage level is seven and the logic stage level is four. Successive path (D) is not a successive compressor critical transistor stage path because for successive path (D) the transistor stage level only is six. However, successive path (D) is a successive compressor critical logic stage path because the logic stage level is four.--

Rewrite paragraph [0053] as follows:

--[0053] A first compressor "critical transistor stage path" may be defined as the path having the greatest transistor stage

level between an input and an output within first compressor 1000. Similarly, a first compressor "critical logic stage path" may be defined as the path having the greatest logic stage level between an input and an output within first compressor 1000. Decreasing the first compressor critical transistor stage path level may increase the speed of the multiplier. Similarly, decreasing the first compressor critical logic stage path level also may increase the speed of the multiplier. However, compressor 1000 may have a plurality of first compressor critical transistor stage paths and a plurality of first compressor critical logic stage paths, or alternatively, may have a single first compressor critical transistor stage path. For ~~Example,~~ example, in compressor 1000, each of path (3) and path (4) is a first compressor critical transistor stage path and also is a first compressor critical logic stage path because for path (3) and path (4) the transistor stage level is six and the logic stage level is three, and no other paths between an input and an output have a greater transistor stage level or a greater logic stage level. Path (1) is not a first compressor critical transistor stage path because for path (1), the transistor stage level only is five, and as such, the transistor stage level for each of path (3) and path (4) is greater than the transistor stage level for path (1). However, path (1) is a first compressor critical logic stage path because the logic stage level for path (1) is three, and as such, the logic stage level for path (1) is the same as the logic stage level for each of path (3) and path (4).--

Rewrite paragraph [0055] as follows:

--[0055] A successive compressor "critical transistor stage path" may be defined as the path having the greatest transistor stage level from one of the inputs of first compressor 1000 to first compressor 1000 carry bit output Xo and further to successive

compressor 1000 summation output So or second carry bit output Co. Similarly, a successive compressor "critical logic stage path" may be defined as the path having the greatest logic stage level from one of the inputs of first compressor 1000 to first compressor 1000 carry bit output Xo and further to successive compressor 1000 summation output So or second carry bit output Co. Decreasing the successive compressor critical transistor stage path level may increase the speed of the multiplier. Similarly, decreasing the successive compressor critical logic stage path level also may increase the speed of the multiplier. However, each compressor 1000 may have a plurality of successive compressor critical transistor stage paths and a plurality of successive compressor critical logic stage paths, or alternatively, may have a single successive compressor critical transistor stage path. For ~~Example,~~ example, in compressor 1000, each of successive path (5) and successive path (6) is a successive compressor critical transistor stage path and also is a successive compressor critical logic stage path because for each of successive path (5) and successive path (6), the transistor stage level is seven and the logic stage level is three. However, successive path (7) is not a successive compressor critical transistor stage path because the for successive path (7) the transistor stage level only is six. However, successive path (7) is a successive compressor critical logic stage path because the logic stage level is three.--